

POWER OF ATTORNEY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ADVANCED MICRO DEVICES, INC., hereby revokes any previous Powers of Attorney and appoints the following attorneys and/or agents in connection with the patent applications and patents identified in Appendix A, owned by ADVANCED MICRO DEVICES, INC., that are filed with the United States Patent and Trademark Office:

each of the practitioners at Customer Number 53806,

as its attorney or agent for so long as they remain with such firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Send all future correspondence to: **Customer Number 53806**

B. Noël Kivlin
Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.
P.O. Box 398
Austin, Texas 78767-0398
(512) 853-8800

Assignee of Interest

ADVANCED MICRO DEVICES, INC.
One AMD Place
P.O. Box 3453
Sunnyvale, CA 94088

Dated: Oct 19, 2009

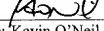
By: 
Name: Kevin O'Neil
Reg. No.: 47,360
Title: Assistant General Counsel

EXHIBIT A

<u>Our Ref.</u>	<u>AMD Ref.</u>	<u>Filing Date</u>	<u>Serial No.</u>	<u>Issued Date</u>	<u>Patent No.</u>	<u>Title</u>	<u>Inventor</u>
5800-33300	F0996	3/23/2001	09/816,706	2/7/2006	6,996,124	Mechanism to Strip LARQ Header and Regenerate FCS to Support Sleep Mode Wake Up	Chow
5800-33400	TT4390	4/19/2001	09/838,652			Determining Logon Status in a Broadband Network System and Automatically Restoring Logon Connectivity	Kyle, Schmidt
5800-33500	F1018	7/2/2002	10/190,088			Method and System for Optimizing the Design of a Network Controller	Gaspar
5800-33600	F1011	3/26/2002	10/107,386			Signaling a Network State Change Among Stations in a Home Phoneline Networking Alliance Media Access Controller (HPNA MAC)	Chow, Karighattam
5800-33700	F1006	12/20/2001	10/028,507			Signal Validation Testing for a Home Phoneline Networking Alliance Media Access Controller (HPNA MAC)	Cooper, Gaspar
5800-33800	C493397	9/29/1997	08/940,691			Method and System for Prevention of Sputtering of a High Conductivity Metal During Via Etch of a Metal Interconnect	Gupta, Chen
5800-33900	H2393	5/15/2007	11/748,743			Methods of Forming Silicides of Different Thicknesses on Different Structures	Yu, Besser, Yang, Yu, Chan
5800-34000	H2406	12/19/2006	11/613,006			Design Rules Checking Augmented with Pattern Matching	Dai, Yang, Rodriguez, Capodieci
5800-34100	H1775	3/1/2004	10/790,590	6/2/2009	7,543,256	System and Method for Designing an Integrated Circuit Device	Lukanc, Tabery, Capodieci, Babcock, Kim, Spence, Haidinyak
5800-34200	NY0128	4/5/2007	11/696,862			Electrically Programmable Reticle and System	Miller
5800-34900	F0857	5/7/2002	09/850706			Method and Apparatus for Monitoring Optical Properties of Anti-Reflective Coatings for Integrated Circuits	Singh, Bhanwar; Hui, Angela T.; Morales, Carmen; Subramanian, Ramkumar

<u>Our Ref.</u>	<u>AMD Ref.</u>	<u>Filing Date</u>	<u>Serial No.</u>	<u>Issued Date</u>	<u>Patent No.</u>	<u>Title</u>	<u>Inventor</u>
5800-35000	H0982	2/5/2004	10/773026	12/25/2007	7312125	Fully Depleted Strained Semiconductor on Insulator Transistor and Method of Making the Same	Xiang, Qi; Besser, Paul R.; Ngo, Minh Van; Paton, Eric N.; Wang, Haihong
5800-35001	H0982DIV	12/6/2007	11/999818			Fully Depleted Strained Semiconductor on Insulator Transistor and Method of Making the Same	Xiang, Qi; Besser, Paul R.; Ngo, Minh Van; Paton, Eric N.; Wang, Haihong
5800-35100	H0960PRV	9/30/2002	60/4515179			SIGE/SI Stack Gate Electrode to Improve NI Polycide for MOSFET	Paton, Eric N.; Xiang, Qi; Besser, Paul R.; Lin, Ming-Ren; Ngo, Minh V.; Wang, Haihong
5800-35102	H0960	12/31/2002	10/335492	9/7/2004	6787864	MOSFETS Incorporating Nickel Germanosilicided Gate And Methods For Their Formation	Paton, Eric N.; Xiang, Qi; Besser, Paul R.; Lin, Ming-Ren; Ngo, Minh V.; Wang, Haihong
5800-35200	H0959 PRV	9/30/2002	60/415,226			FINFET Device Incorporating Strained Silicon In The Channel Region	Lin, Ming-Ren; Goo, Jung-Suk; Wang, Haihong; Xiang, Qi
5800-35201	H0959	12/31/2002	10/335474	10/5/2004	6800910	FINFET Device Incorporating Strained Silicon In The Channel Region	Lin, Ming-Ren; Goo, Jung-Suk; Wang, Haihong; Xiang, Qi
5800-35300	H1725	2/2/2004	10/769835	4/29/2008	7364962	Shallow Trench Isolation Process Utilizing Differential Liners	Krishnan, Srinath

<u>Our Ref.</u>	<u>AMD Ref.</u>	<u>Filing Date</u>	<u>Serial No.</u>	<u>Issued Date</u>	<u>Patent No.</u>	<u>Title</u>	<u>Inventor</u>
5800-35301	H1725DIV	3/13/2008	12/047636			Shallow Trench Isolation Process Utilizing Differential Liners	Krishnan, Srinath
5800-35302	H1725DIV-CNT	8/7/2009	12/538,008			Shallow Trench Isolation Process Utilizing Differential Liners	Krishnan, Srinath
5800-35400	H1731	9/3/2003	10/654631	7/18/2006	7078299	Formation Of FINFET Using A Sidewall Epitaxial Layer	Maszara, Witold P.; Goo, Jung-Suk; Pan, James N.; Xiang, Qi
5800-35500	F0822	6/25/2001	09887035	10/12/2004	6803178	Two Mask Photoresist Exposure Pattern For Dense And Isolated Regions	Subramanian, Ramkumar; Bell, Scott A.; Lukanc, Todd P.; Plat, Marina V.; Okoroanyanwu, Uzodinma; Kim, Hung-Eil
5800-35501	F0822DIV	8/24/2004	10/925123	5/6/2008	7368225	Two Mask Photoresist Exposure Pattern For Dense And Isolated Regions	Subramanian, Ramkumar; Bell, Scott A.; Lukanc, Todd P.; Plat, Marina V.; Okoroanyanwu, Uzodinma; Kim, Hung-Eil
5800-35600	H2175	4/4/2005	11/098262	5/26/2009	7538026	Multilayer Low Reflectivity Hard Mask And Process Therefor	Ghandehari, Kouroos; Minvielle, Anna M.; Plat, Marina V.; Tokuno, Hirokazu
5800-35601	H2175DIV	5/19/2009	12/468715			Multilayer Low Reflectivity Hard Mask And Process Therefor	Ghandehari, Kouroos; Minvielle, Anna M.; Plat, Marina V.; Tokuno, Hirokazu